ParSec: Ein paralleles und sicheres drahtloses Kommunikationssystem für die Fertigungssteuerung

Rolf Kraemer

innovations
for high
performance
microelectronics

9.05.2017

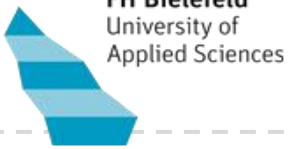
kraemer@ihp-microelectronics.com

Member of Leibniz Association

Consortium


innovations
for high
performance
microelectronics


Brandenburgische
Technische Universität
Cottbus - Senftenberg


FH Bielefeld
University of
Applied Sciences


HUMBOLDT-UNIVERSITÄT ZU BERLIN


technische universität
dortmund


BOSCH


Rexroth
Bosch Group


escrypt
Embedded Security


HARTING


imst
Design + Systems International GmbH


WAGO
INNOVATIVE CONNECTIONS

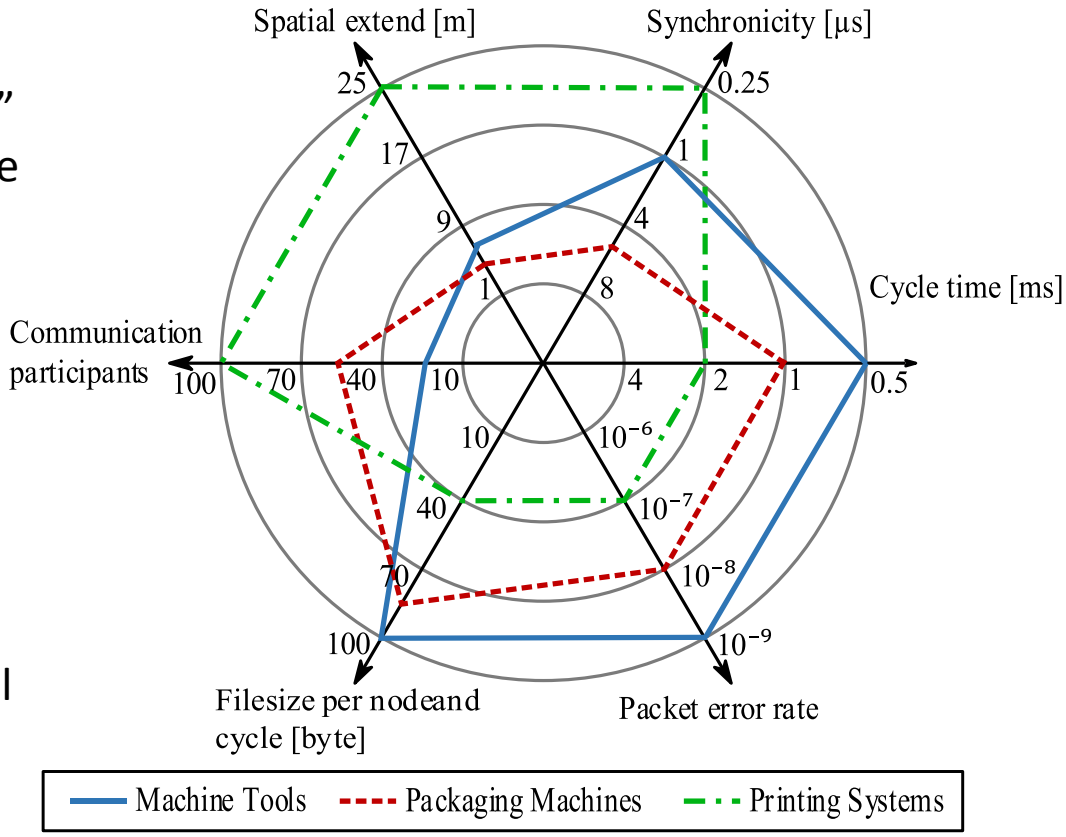

NXP

Outline

Introduction

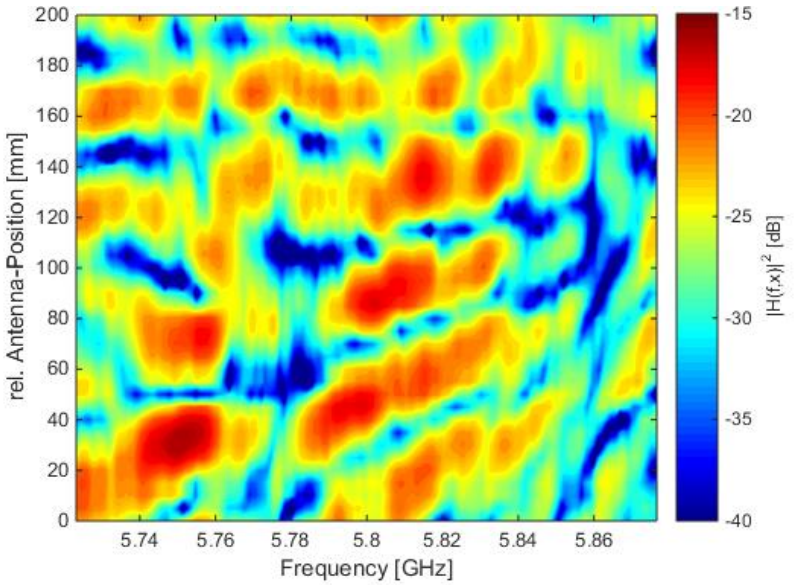
- Wireless systems today are not useable for hard real-time control of automation processes
- Latency and error rate are to high
- Security is to low
- Field-bus systems are “closed-loop” systems with a constant frame-time

- ParSec introduces a new concept for highly parallel communication with guaranteed latency of < 1ms within a manufacturing cell
- Error rate should come close to 10^{-9} based on channel-coding
- Embedded Security is optimized to short packages as used in industrial control
- A rapid prototype of a full radio for closed-loop operation has been used for channel measurement and implementation



Challenges

- The wireless channel in industrial environments is particular bad due to several strong reflectors and attenuators
- Break-In of ≥ 40 dB occur frequently in short geometrical distances
- The pattern is highly frequency dependent



- We need a radio that allows to mitigate the deep interference effects by using high bandwidth (≥ 200 MHz)

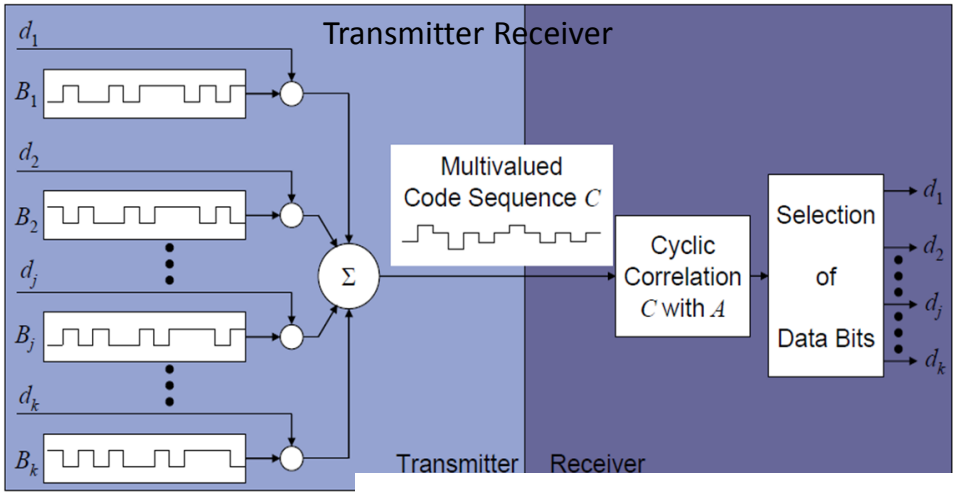
- Access to the wireless medium in ISM-band is usually performed by “listen before talk” (CSMA/CA is the most commonly used access protocol)
- “Listen before talk” prohibits hard-real-time guarantees
- A band for industrial control is necessary to solve this problem (14 dBm emission is permitted for access without “listen before talk” restricting to size of the covered control cell significantly)

Introduction to PSSS

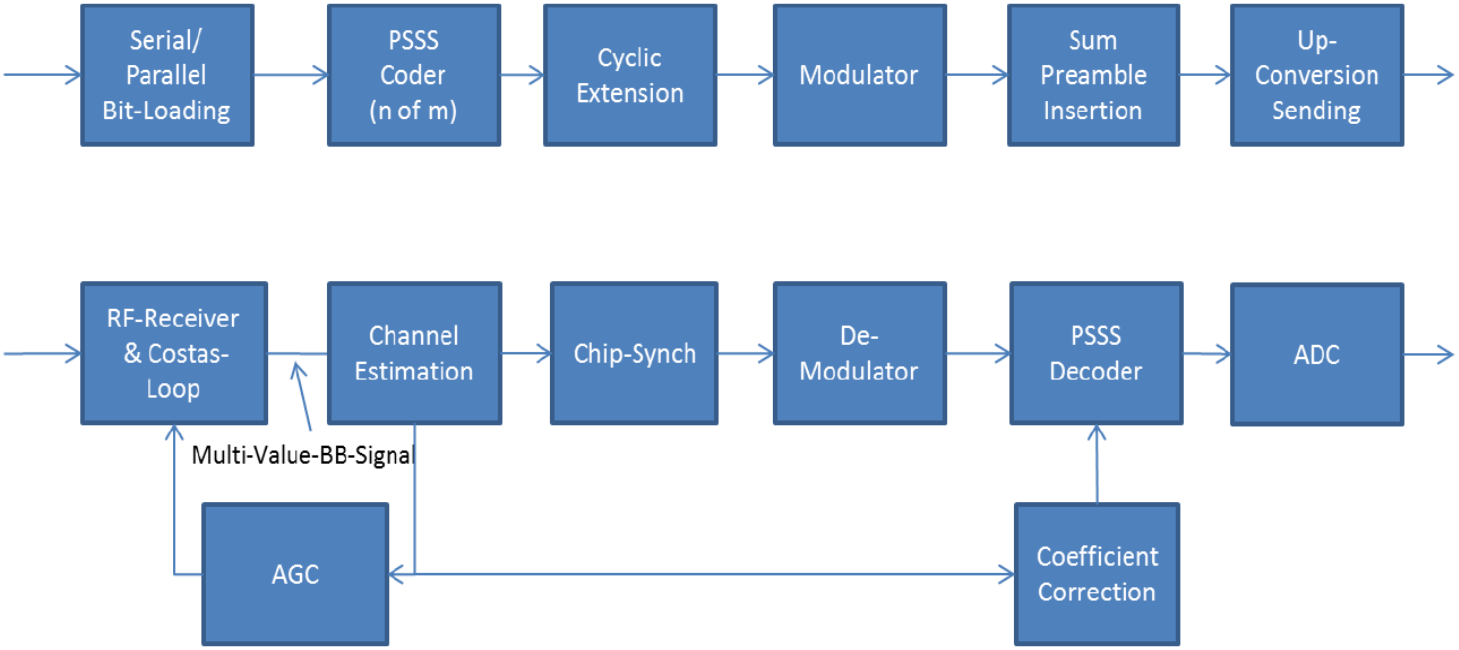
- PSSS is a spread-spectrum technique allowing parallel transmission using orthogonal codes
- The code length can by widely adapted to the needs of the target application and the available spectrum
  - For ParSec we choose a PSSS-code length of 255 chips
- The symbol rate determines the necessary bandwidth
  - For ParSec we choose a symbol rate of 71.5 kHz resulting in a bandwidth of 20 MHz
- The maximal data rate (without FEC and @ 1 b/s/Hz) is 15 Mb/s

- Other impotant figures:
  - Symbol duration: 14 µs
  - Chip duration: 55 ns

PSSS System approach



- PSSS uses orthogonal m-sequences
- The signal can be further modulated e.g. using PAM
- The receiver correlates, integrates and de-modulates the signal

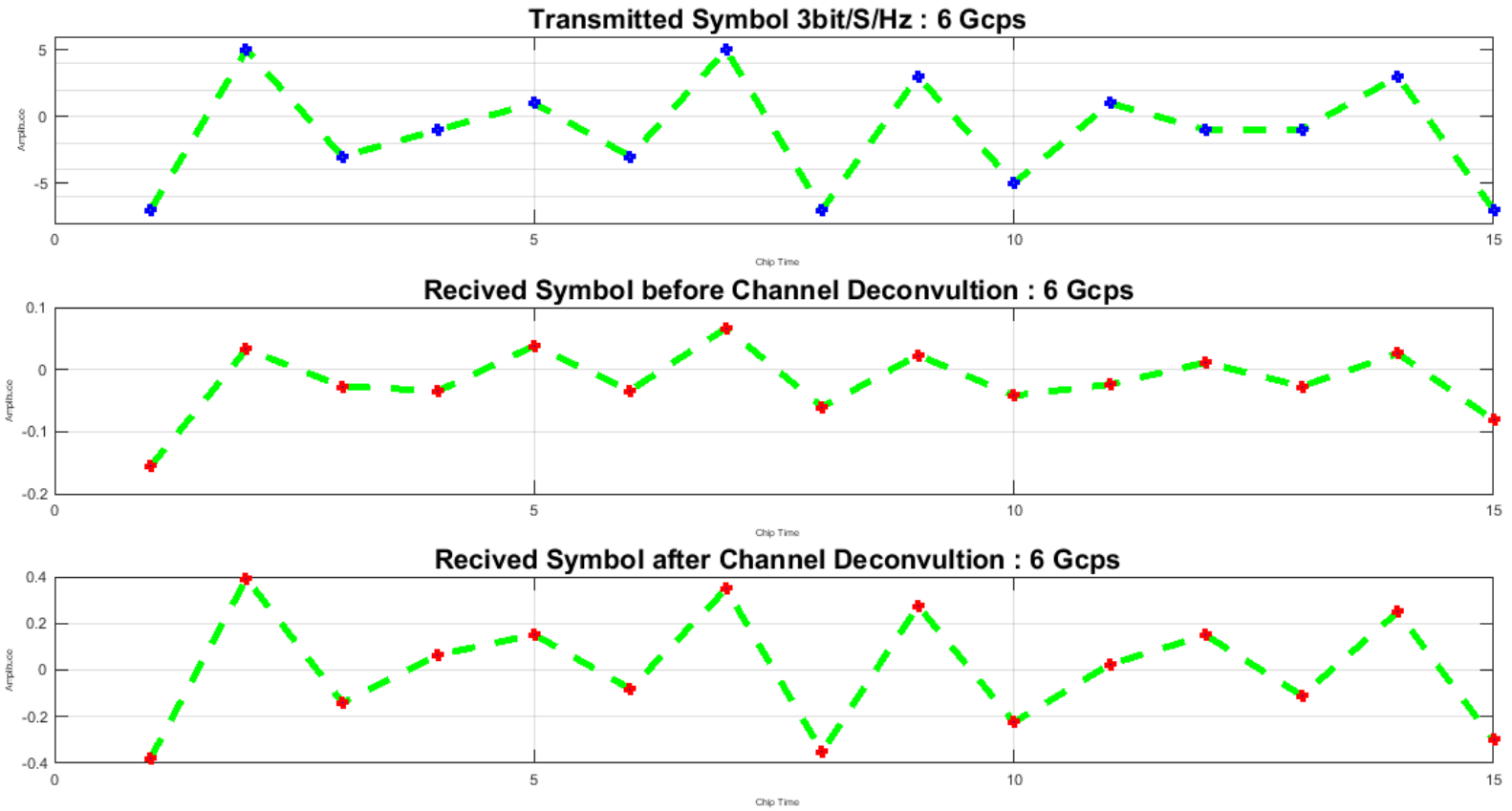


Closed Loop System (down-link)

- The ParSec System will be used within a closed-loop system, e.g. a „field-bus
- The system will run in FDD-mode, thus the down-link and up-link use independent frequencies
- In down-link direction every client can make it's own receive control
  - The de-convolution with the channel impairments leads to a very effective channel compensation
  - We correct the effective channel, i.e. including the RF-impairments
  - Synchronization and AGC is client controlled based on master clock and distance between master and client

Effect of channel de-convolution/correction on signal quality

Measurements have been taken from DFG-Projekt: Real100Gcom using only 15 chip PSSS code but quite high symbol rate and bandwidth



Closed-loop system (up-link)

- Due to the reception of the compound signal of all clients up-link three problems have to be solved:
  - Channel de-convolution (using pre-distortion)
  - Chip synchronization (using time-advance)
  - Fast-power-control (using client-uplink power control)

- Channel de-convolution
  - To allow a channel estimation of the up-link channel in each client, the master send a number of training-symbols on uplink frequency in downlink direction within each frame. These symbols are used by the clients to make up-link channel estimation.
  - Based on the up-link channel estimation each client pre-distorts (convolutes) the uplink signal with the invers channel vector.
  - Thus the master receives the channel compensated signal

- Chip-synchronization

Closed-loop system (up-link)

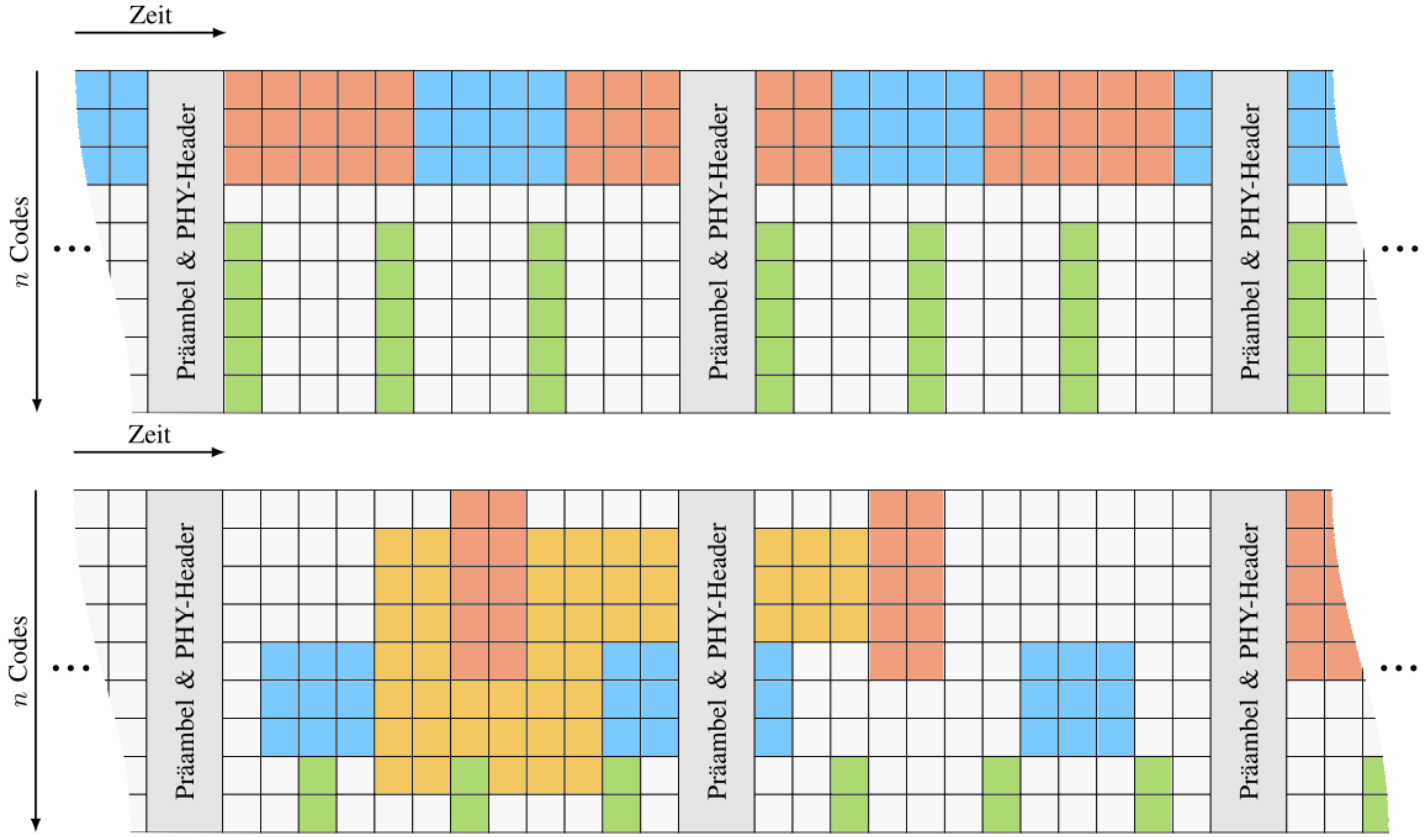
- Chip-synchronization
  - The clients are in different distances with respect to the master.
  - To allow for correct chip-synchronization (important for the cyclic-correlation) each client sends the uplink signal distance corrected.
  - If we allow for a synchronization mismatch of ¼ chip we need an accuracy of <15 ns (corresponding to 5m distance difference)
  - The master measures the relative distance between clients and sends the a correction value in downstream to each client with each frame.
  - The correction value is used as “time-advance” signal, i.e. the clients that are further away send their signals earlier than the clients close to the master.
- Power-control
  - The receive-power plays an essential role for the cyclic correlation process on the master side.
  - To avoid big differences in receive-power due to different channels and distances to master sends power correction signal with each frame to each client

Field-Bus synchronization

- Basically the clocks of the field-bus system and the wireless system are de-coupled.
- To avoid synchronization problems ParSec is synchronized to the 1MHz field-master clock.
- The field master clock triggers the ParSec Frame emission with a 1 kHz clock
- The frame length is < 1ms such that we can transmit the frame quasi asynchronously
- ParSec assures the full frame delivery in synchronization with the field master.

Resource-block organization

- Logical Transmission in ParSec is organized in Frames
- Frames consist of a frame header for training symbols and individual resource blocks for each clients (downlink) or up-link resource block from each client.
- The smallest resource block contains 1-4 bit (according to the chosen modulation)
- The initial ParSec system will support 1 bit resource blocks

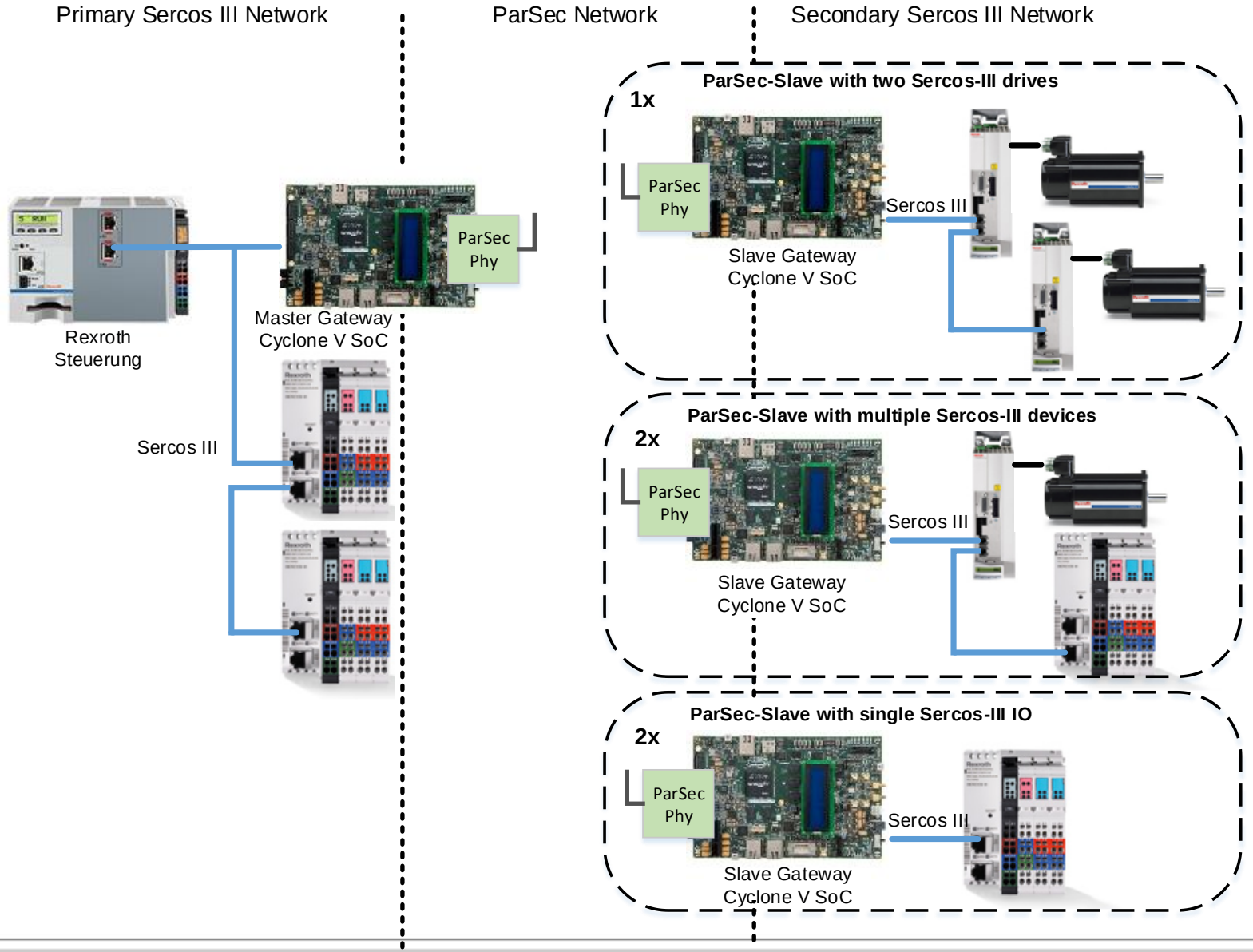


ParSec Rapid Prototype

- Consisting of 3 boards:
- BeagleBone processor board for MAC and Field Bus interface
- FPGA board implementing PSSS-255 digital baseband
- RF board with commercial AD-9361 frontend chip @ 5.7 GHz

- Rapid prototype shall be used to investigate ParSec Radio System under real-time conditions in real industrial environments.
- FPGA and AD-9361 are to be replaced by ParSecS ICs developed by IMST and IHP.

Planned Demonstrator (High-End System)



Conclusion

- The presented work is „work in progress“

- We have a working closed loop system for initial experiments and measurements
- The RF-Frontend-chip has been designed and a first tape-out was in Q1-2017
- The MAC-implementation is ongoing

- With ParSec we intend to cover essential problems of wireless control with hard real-time conditions. The chosen 1ms latency will be good, but for solving also all high-end system requirements we need to come to < 250 µs. This is possible with the ParSec approach but currently not compatible to the wired field-bus systems.

- Not all problems will be solved due to missing regulations:
  - Bandwidth limitation and power limitation
    - Even if 150 MHz bandwidth will be granted the deep fading problem cannot be solved without additional measures
    - ParSec basically can use longer codes (e.g. 1023 long). This would reduce the number of parallel cells
- As an ParSec extension we are currently also investigating a “COMP” approach to solve the deep fading problem with limited bandwidth.

Acknowledgement

ParSec is part of the BMBF initiative „ZDKI“. It is funded under this program. We would like to thank the ministry for the financial support

We also would like to thank all partners of the consortium for the constructive cooperation

Thank you for your attention!

innovations
for high
performance
microelectronics

IHP – Innovations for High Performance Microelectronics
Im Technologiepark 25
15236 Frankfurt (Oder)
Germany
Phone: +49 (0) 335 5625
Fax: +49 (0) 335 5625
Email:

www.ihp-microelectronics.com

Member of Leibniz Association